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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,693	12/03/2001	Hirotaka Ito	60188-123	6650

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EXAMINER	
MATTIS, JASON E	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,693	ITO ET AL.	
	Examiner	Art Unit	
	Jason E. Mattis	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no avent, however, may a raply ba timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within tha statutory minimum of thirty (30) days will ba considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statuta, causa tha application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-10 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 03 December 2001 is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/01, 4/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 9-11 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by Williams (U.S. Pat. 6205494).

With respect to claim 10, Williams discloses a multi-initiator control method for performing packet-unit communication with each of a plurality of devices connected via a transmission line **(See column 1 lines 17-23, column 6 lines 24-58, and Figure 8 of Williams for reference to a command queuing means CQE 800, which is a multi-initiator controller located in a target device, using a control method and for reference multiple initiators and targets being connected by a SCSI bus)**. Williams also discloses determining whether or not receipt of a command fetch request from one of the plurality of devices is stored and fetching a command from the device and executing the command when it is determined that receipt of a command fetch request is stored **(See column 6 line 59 to column 7 line 17 of Williams for reference to determining if a DTD 600, which is a command entry, is stored and fetching and performing the command if a DTD 600 is found while waiting for a new DTD 600 to be received if no more DTDs 600 are found)**. Williams further discloses that one of the devices is selected in a predetermined order to perform the step of determining and the step of fetching with the process being repeated **(See column 6 line 59 to column 7 line 17 and Figures 5 and 8 of Williams for reference to selecting a device command, DTD 600, in a predetermined order by selecting linked consecutive DTDs 600 first before selected a non-linked new DTD 600, with each DTD corresponding to a device as indicated in the initiator device field of the of the entry stored in the command registers 830, as shown in Figure 5)**.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Williams.

With respect to claim 1, Applicant's admitted prior art discloses an initiator control unit **(See page 7 lines 21-22 and Figure 11 of Applicant's specification for reference to sequence processor 90, which is an initiator control unit)**. Applicant's admitted prior art also discloses a link core circuit for transmitting a packet to the transmission line and receiving a packet from the transmission line, performing error detection, and outputting the error-detected packet **(See page 7 line 25 to page 8 line 6 and Figure 11 of Applicant's specification for reference to a link core circuit 92 receiving and transmitting packets while performing error detection)**. Applicant's admitted prior art further discloses a packet filter for analyzing the packet received by the link core circuit and outputting the results **(See page 8 lines 9-15 and Figure 11 of Applicant's specification for reference to a packet filter 93 that analyzes the content of packet header fields and sends outputs a signal depending on the result of the analysis)**. Applicant's admitted prior art also discloses a packet processing circuit for generating a packet containing information output by a command

control circuit to be transmitted an outputting the packet according to analysis results of the packet filter **(See page 8 lines 11-19 for reference to packet processing circuit 95 generating and outputting a packet according to information received from the packet filter 93)**. Applicant's admitted prior art further discloses a CPU for executing a command contained in the packet **(See Figure 11 of Applicant's admitted prior art for reference to CPU 31, which executes a command as output by the packet processing circuit 95)**. Applicant's admitted prior art does not disclose that the control unit is a multi-initiator control unit. Applicant's admitted prior art also does not disclose a plurality of command control circuits for controlling a command processing sequence. Applicant's admitted prior art further does not disclose a multi-control circuit for giving sequence execution permission to one of the command control circuits.

With respect to claim 1, Williams, in the field of communication, discloses a multi-initiator control unit **(See column 1 lines 17-23, column 6 lines 24-58, and Figure 8 of Williams for reference to a command queuing means CQE 800, which is a multi-initiator controller located in a target device, using a control method and for reference multiple initiators and targets being connected by a SCSI bus)**. Williams also discloses a plurality of command control circuits for controlling a command processing sequence **(See column 6 lines 24-58 and Figure 5 and 8 of Williams for reference to command registers 830 and DTD buffer 850, which together perform the function of a plurality of command control circuits by storing information in the command registers and DTD buffer relating to commands that have been received from devices corresponding to the initiator**

field stored in the registers). Williams further discloses a multi-control circuit for giving sequence execution permission to one of the command control circuits **(See column 6 line 24 to column 7 line 17 and Figures 8-9 of Williams for reference to interface processor 84 and DTDG 820, which together perform the function of a multi-control circuit by using command information to determine the sequence in which interface processor issues GO commands to process and execute commands stored based on the outcome of the DTDG 820)**. Using a multi-initiator control unit with a plurality of command control circuits and a multi-control circuit has the advantage of allowing multiple commands sent by multiple initiators to be stored and subsequently processed in an efficient manner.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Williams, to combine using a multi-initiator control unit with a plurality of command control circuits and a multi-control circuit, as suggested by Williams, with the system described by the Applicant's admitted prior art, with the motivation being to allow multiple commands sent by multiple initiators to be stored and subsequently processed in an efficient manner.

With respect to claim 2, Applicant's admitted prior art discloses the packet processing circuit generating a packet containing information output by a command control circuit provided with execution permission and outputting the packet, and receiving a packet output by the corresponding device in response to the packet output by the packet processing circuit **(See page 8 lines 11-19 for reference to packet processing circuit 95 generating and outputting a packet according to**

information received from the packet filter 93). Applicant's admitted prior art does not disclose the command control circuits storing information required for command processing output by a corresponding device and outputting the information once the sequence execution permission is given. Applicant's admitted prior art also does not disclose the multi-control circuit outputting information to the command control circuit based on the output of the packet filter.

With respect to claim 3, Applicant's admitted prior art does not disclose that the command control circuits store information in a command fetch request packet and performs the command fetch operation once execution permission is given.

With respect to claims 2-3, Williams discloses the command control circuits storing information required for command processing output by a corresponding device and outputting the information once the sequence execution permission is given **(See column 6 line 5 to column 7 line 17 and Figures 5 and 8 of Williams for reference to storing information required for command processing output by a device in both the command register file 830, with the information being stored based on the initiator that send the command, and in the DTD buffer 850, as DTDs, which are command fetch request packets. and for reference to outputting a DTD from the DTD buffer when a GO command, or fetch permission command, is issued to fetch the command)**. Williams also discloses the multi-control circuit outputting information to the command control circuit based on the output of the packet filter **(See column 7 lines 24-58 and Figure 8 for reference to the DTDG 820 using information in the incoming commands to determine how and where to output the**

incoming commands to the DTD buffer 850). Using the multi-control circuit to determine how and where to store command information in the command control circuits has the advantage of preprocessing each command so that they are stored in the appropriate area such that they commands may be executed in the most efficient order.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Williams, to combine using the multi-control circuit to determine how and where to store command information in the command control circuits, as suggested by Williams, with the system described by the Applicant's admitted prior art, with the motivation being to preprocess each command so that they are stored in the appropriate area such that they commands may be executed in the most efficient order.

With respect to claim 4, the Applicant's admitted prior art does not disclose the command control circuits receiving a command fetch request during execution of a data transfer processing sequence.

With respect to claim 4, Williams discloses command control circuits receiving a command fetch request during execution of a data transfer processing sequence **(See column 6 line 24 to column 7 line 17 of Williams for reference to the storing of commands in the command register file 830 and the DTD buffer 850 being and independent and current process to that of executing commands, meaning commands are received during execution of prior received commands)**. Having command control circuits receive a command fetch request during execution of a data

transfer processing sequence has the advantage of allowing commands to be received and stored at any time, such that newly received commands are not blocked during the execution of previously received commands.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Williams, to combine having command control circuits receive a command fetch request during execution of a data transfer processing sequence, as suggested by Williams, with the system described by the Applicant's admitted prior art, with the motivation being to allow commands to be received and stored at any time, such that newly received commands are not blocked during the execution of previously received commands.

With respect to claim 6, the Applicant's admitted prior art does not disclose the multi-control circuit selecting one of the plurality of devices in a predetermined order every time a command processing sequence is terminated and giving permission to execute the selected device command.

With respect to claim 6, Williams discloses the multi-control circuit selecting one of the plurality of devices in a predetermined order every time a command processing sequence is terminated and giving permission to execute the selected device command **(See column 6 line 59 to column 7 line 17 and Figure 8 of Williams for reference to selecting a next DTD 600 in a predetermined order after the completion of a previous selected DTD 600 and giving permission to execute the next selected DTD 600)**. Having the multi-control circuit select one of the plurality of devices in a predetermined order every time a command processing sequence is

terminated and giving permission to execute the selected device command has the advantage of allowing the commands to be selected in the most efficient manner each time a previously selected command has been executed.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Williams, to combine having the multi-control circuit select one of the plurality of devices in a predetermined order every time a command processing sequence is terminated and giving permission to execute the selected device command, as suggested by Williams, with the system described by the Applicant's admitted prior art, with the motivation being to allow the commands to be selected in the most efficient manner each time a previously selected command has been executed.

With respect to claim 7, Applicant's admitted prior art discloses a transfer control circuit for controlling data transfer between the packet processing circuit and the outside of the control unit **(See page 8 lines 15-19 of Applicant's specification for reference to the transfer control circuit 96)**. Applicant's admitted prior art also discloses that the packet processing circuit retrieves data and outputs data to the transfer control circuit and also generates a packet containing data transferred to the transfer control circuit and outputs the packet to the link core circuit **(See page 8 lines 15-21 for reference to the packet processing circuit 95 performing this process)**.

With respect to claim 8, Applicant's admitted prior art does not disclose that the CPU is allowed to give sequence execution permission.

With respect to claim 8, Williams discloses the CPU giving sequence execution permission **(See column 6 line 59 to column 7 line 17 of Williams for reference to processor 84 initiating a command sequence by sending a GO command)**. Having the CPU give sequence execution permission has the advantage of allowing the device processing commands, which can determine when a command is finished being processed, to determine when to fetch a new command to be processed.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Williams, to combine having the CPU give sequence execution permission, as suggested by Williams, with the system described by the Applicant's admitted prior art, with the motivation being to allow the device processing commands, which can determine when a command is finished being processed, to determine when to fetch a new command to be processed.

With respect to claim 9, the Applicant's admitted prior art does not disclose that correspondence is established between the node number of each of the devices and the position of a bit field for identification of the node number.

With respect to claim 9, Williams discloses a correspondence established between the node number of each of the devices and the position of a bit field for identification of the node number **(See column 1 lines 42-62 and Figure 1 of Williams for reference to using a three-bit logical unit number to address devices, or nodes)**. Establishing a correspondence between the node number of each of the devices and the position of a bit field for identification of the node number has the advantage of providing a simple way to address host or initiator devices.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Williams, to combine establishing a correspondence between the node number of each of the devices and the position of a bit field for identification of the node number, as suggested by Williams, with the system described by the Applicant's admitted prior art, with the motivation being to provide a simple way to address host or initiator devices.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Williams as applied to claims 1-4 and 6-9 above, and further in view of Bashford et al. (U.S. Pat. 6529989).

With respect to claim 5, Williams discloses the command control circuits having register for storing an address for performing a command processing sequence **(See column 6 lines 24-58 and Figures 5 and 8 of Williams for reference to command registers 830 for storing an address for performing a command processing sequence)**. The combination of Applicant's admitted prior art and Williams does not disclose that an address register is obtained by performing address expansion on an address of the register of a reference command control circuit depending on the node number of a device.

With respect to claim 5, Bashford et al., in the filed of communications, discloses performing address expansion on an address depending on a node number of a device **(See column 4 line 60 to column 5 line 6 and column 6 lines 15-47 of Bashford et al. for reference to performing address expansion to store**

information). Performing address expansion on an address depending on a node number of a device has the advantage of allowing a larger number of devices to send commands to a target.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Bashford et al., to combine performing address expansion on an address depending on a node number of a device, as suggested by Bashford et al., with the system described by the Applicant's prior art and William, with the motivation being to allow a larger number of devices to send commands to a target.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Krakirian et al. (U.S. Pat. 5781803) discloses a multi-initiator system and method. Ellis et al. (U.S. Pat. 594806) discloses a method of controlling a target in a multi-initiator system. Ellis et al. (U.S. Pat. 6112278) discloses a method of storing initiator information. Reynolds et al. (U.S. Pat. 6138161) discloses a multi-initiator system and method. Born et al. (U.S. Pat. 6247040) discloses a method for switching between contexts in a target device. Basham (U.S. Pat. 6430645) discloses address mapping for multiple initiator support. Reynolds et al. (U.S. Publication US 2004/0170432 A1) discloses a method and system for multi-initiator support.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason E. Mattis whose telephone number is (571) 272-3154. The examiner can normally be reached on M-F 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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